Received: 30 September 2023 | Revised: 29 December 2023 | Accepted: 18 January 2024

IET Power Electronics

DOI: 10.1049/pel2.12665

The Institution of Engineering and Technology WILEY

ORIGINAL RESEARCH

Capacitor sizing of three-level neutral point clamped voltage source inverter for electric vehicles: Effects of modulation and motor characteristics

Serhat Emir Ogan | **Emine Bostanci**

Electrical and Electronics Engineering Department, Middle East Technical University, Ankara, Turkey

Correspondence
Emine Bostanci, Electrical and Electronics Engineering Department, Middle East Technical University, Ankara 06800, Turkey.
Email: emineb@metu.edu.tr

Funding information
Scientific and Technological Research Council of Turkey, Grant/Award Number: 121E729

Abstract

A three-level neutral point clamped (3L-NPC) voltage source inverter (VSI) topology can be advantageous in electric vehicles with a high DC-link voltage and a high switching frequency. A bulky DC-link capacitor is not an option; thus, the DC-link capacitor's sizing considering the traction system characteristics is an important design step. This paper investigates how the DC-link capacitor size of a 3L-NPC VSI gets affected by the combination of the interdependent characteristics of an electric drive, such as its power factor, modulation index, current, and fundamental frequency, with the effects of the modulation methods. Five pulse width modulation (PWM) methods, of which three of them have an active neutral point potential control, are compared in terms of their neutral point potential (NPP) oscillations. Then, the size of the DC-link capacitor is determined for each PWM method so that the NPP ripple is kept under desired limits at all operating conditions. It is shown that both the modulation technique and the electric machine characteristics influence the capacitor size. For example, electric machine design modifications can introduce more than a 30% reduction in capacitor size. Finally, DC-link and NPP oscillations with different PWM methods are experimentally validated in a scaled-down 3L-NPC inverter.

1 | INTRODUCTION

The expanding electric vehicle (EV) market raises interest in designing EV traction systems with higher power density and efficiency. Common approaches to achieve these goals involve increasing the rotational speed of the traction electric machine and the DC-link voltage levels [1]. Increasing the DC-link voltage level is considered a potential solution to reduce battery charging times [1]. For instance, both Porsche and Fisker have proposed the use of an 800 V DC-link voltage level to achieve shorter charging times [2].

Two-level three-phase voltage source inverters (VSIs) with a DC-link voltage of approximately 300–400 V are commonly employed in EVs [2]. However, DC-link voltages of 800 V or higher necessitate a traction inverter with a correspondingly higher rated input voltage, given that the traction inverter and the battery system are typically connected to the same DC bus in most EVs. To satisfy the need for an increased speed and higher DC-link voltage, a three-level neutral point clamped (3L-NPC) voltage source inverter (VSI) shown in Figure 1 is seen as a good alternative topology.

Semiconductors in the 3L-NPC inverter block half of the DC-link voltage; hence, the 3L-NPC becomes more attractive with increasing DC-link voltage [2]. Furthermore, it is a preferable alternative when using gallium nitride-based (GaN-based) semiconductor devices, as this technology can only provide limited blocking voltage. 3L-NPC topology is also preferable because of its lower switching losses compared to a two-level VSI [3, 4]. This feature supports the increase in the maximum fundamental frequency of the drive system [5, 6]. Another benefit of the 3L-NPC VSI is its lower total harmonic distortion, which is advantageous for reducing the core losses in the electric machine [4, 7].

A crucial drawback of the 3L-NPC VSI is the requirement for neutral point potential (NPP) control. Phase currents connected to the neutral point deplete one capacitor while charging the

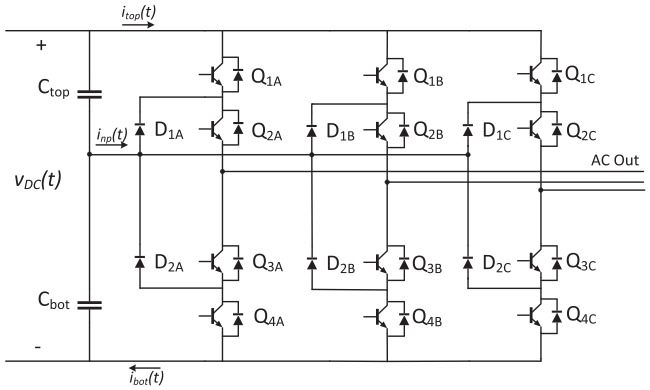

FIGURE 1 Three-level neutral point clamped inverter topology.

other. This asymmetrical use of the capacitor charge results in a voltage ripple at the neutral point of the inverter [2, 8]. Therefore, a low-frequency voltage ripple is observed at the neutral point of a 3L-NPC VSI in addition to a ripple at the switching frequency and its side bands. If left unaddressed, NPP ripple may lead to high voltages across the power switches, potentially shortening their lifetime and causing permanent damage. Furthermore, NPP control is crucial to limit the DC-link capacitor losses [3].

The most straightforward way to limit the NPP ripple is to increase the size of the DC-link capacitors. However, this leads to a high volume and additional weight of the DC-link capacitor for constant frequency applications, and more importantly, it is not appropriate for variable frequency applications. As a result, numerous studies focus on NPP ripple control methods, wherein the switching states and duty cycles of semiconductors are adjusted to reduce the NPP ripple [9]. Due to the importance of the problem, novel pulse width modulation (PWM) methods are proposed to reduce the NPP ripple in several recent publications, such as in [10–13].

NPP ripple is expected to increase proportionally with phase current and inversely proportional with the fundamental output frequency and DC-link capacitance. However, the ability of PWM methods to reduce NPP ripple varies based on power factor and modulation index. In [14], the authors analyse capacitor currents and state the analytical relationship between power factor, modulation index, and DC-link capacitor current. Jain et al. [15] compare popular PWM methods in terms of their NPP ripple. Moreover, in [16], analysis of neutral point current has been conducted for 3L-NPC VSIs using various PWM methods to determine the appropriate capacitor size. However, the capacitor sizes are determined for a grid-connected PV inverter application, which has constant frequency and different load characteristics compared to a variable-speed drive application.

In a motor drive application, the main operation parameters of the inverter, for example, modulation index, power factor, load current, and frequency, are determined by the motor characteristics. Therefore, the traction motor has a significant effect on the NPP ripple. In [17], Masisi et al. explore the change in the DC-link capacitor size of a 3L-NPC inverter as a function of the magnetic saliency difference between the *d*- and *q*-axes of a synchronous reluctance machine for a specific PWM method. The magnetic saliency mainly affects the power factor and, thus, the capacitor size. However, apart from looking into a single PWM method, a comprehensive relationship between the motor characteristics and the NPP ripple is not analysed.

This study aims to investigate the impact of electric machine characteristics and PWM methods on the DC-link capacitor sizing of a 3L-VSI within the context of a specific EV traction drive application. The development of a novel NPP ripple control method is beyond the scope of this study. A permanent magnet-assisted synchronous reluctance machine (PMaSynRM) drive is chosen based on recent trends. The sizing of DC-link capacitors is performed for five different PWM methods. Two of the selected PWM methods have no NPP control: that are sinusoidal PWM (SPWM) and space vector PWM (SVPWM). The other three selected PWM methods have NPP control: that are the nearest triangle vector (NTV) method, the symmetric space vector PWM (symmetric SVPWM) method proposed in [18] and the equal O-state method proposed in [19].

This study shows that the electric drive's most critical operating point concerning 3L-VSI NPP ripple highly varies with electric machine characteristics and the chosen PWM method. Such analyses and comparisons are not present in the literature. The further findings of this study can be summarized below:

- In contrast to two-level inverters, sizing DC-link capacitors for 3L-NPC inverters requires consideration of both switching frequency harmonics and low-frequency harmonics. Consequently, the pole number inversely influences the DC-link capacitor size of a 3L-NPC VSI in most PWM methods.
- PWM methods with uncontrolled NPP ripple, such as sinusoidal PWM and space vector PWM, are unsuitable for low-speed and high-torque operation regions in variable-speed applications. This study explains modifications to these PWM methods to mitigate excessive ripple at the mentioned operating points.
- Minor adjustments in the power factor of the electric machine within high modulation index regions can significantly impact NPP ripple and, consequently, the DC-link capacitor size.

The rest of the paper is organized as follows: Investigated PWM methods are introduced and explained in Section 2. A low-frequency NPP ripple model is adjusted for all five PWM methods, and the results of this model are used to determine the effect of output frequency, modulation index, phase current, and power factor on the NPP ripple in Section 3. The characteristics of the selected reference drive are introduced, and operating points with the largest possible low-frequency NPP ripple are identified in Section 4. Then, capacitor sizing for the motor drive application is completed for the 3L-NPC topology in Section 5. The study points out an unbounded NPP ripple problem with sinusoidal and space vector PWM methods at very low frequencies and a solution for this problem is emphasized in Section 6. The influence of the machine's pole number and power factor on the capacitor size is discussed in Section 7. Finally, findings are experimentally supported in Section 8,

DC-link capacitor sizing is also performed for the 2L-VSI topology in Section 9, and conclusions are given in Section 10.

2 | PWM METHODS

The five selected PWM methods are described in this section. Two of the chosen PWM methods, namely SPWM and SVPWM, do not employ NPP control. In other words, the gate signals of power switches are not influenced by NPP. Three of the selected PWM methods, namely NTV, symmetric SVPWM, and the equal O-state method as described in [19], incorporate NPP control. Therefore, the gate signals of the inverter switches are determined based on the NPP level.

2.1 | Sinusoidal pulse width modulation (SPWM)

In this method, phase-to-neutral point voltages are determined based on the voltage reference signals and two triangular carrier waves. Voltage reference signals are scalar quantities that vary between [−1, 1]. On the other hand, triangular carrier waves have variable values between [0, 1] and [−1, 0]. Both carrier-wave signals have a frequency equal to the switching frequency (f_{sw}) of the inverter.

Different phase to neutral point voltages are obtained with different switch positions. When the voltage reference signal of one phase is larger than both carrier wave signals, the top two power switches (Q1, Q2) are turned on while the bottom two switches (Q3, Q4) are turned off. In this case, voltage $\frac{V_{DC}}{2}$ is applied to phase to neutral point voltage of the corresponding phase. When the voltage reference signal is larger than one carrier wave and smaller than the other, the middle two switches (Q2, Q3) are turned on while the other two switches (Q1, Q4) are turned off. Phase to neutral voltage is 0 in this particular case for the corresponding phase. In the last case, the voltage reference signal is smaller than both carrier wave signals. The bottom power switches (Q3, Q4) are turned on while the top power switches (Q1, Q2) are turned off. Phase to neutral voltage is applied as $-\frac{V_{DC}}{2}$.

The main advantage of the SPWM method is its simplicity. However, a high NPP ripple is expected because there is no NPP control with this method. Another disadvantage is having a limited modulation index. Modulation index m_i is defined as the proportion of peak phase voltage to half of the DC-link voltage. In the SPWM method, the maximum modulation index is limited to one, while in the other PWM methods, modulation indexes larger than one can be applied.

2.2 | Space vector pulse width modulation (SVPWM)

In this study, space vector pulse width modulation is applied as provided in [20]. In this PWM method, the switch state of each phase is expressed with P, O or N. Then, every possible switch position is placed on the space vector diagram according to its magnitude and phase. The resulting space vector diagram is shown in Figure 2. The voltage reference vector is placed on the space-vector diagram according to its magnitude and phase. Depending on the position of the voltage reference vector, four vectors are selected to express the voltage reference vector as a vector summation of four vectors. The coefficients of the voltage vectors determine the dwell time of each voltage vector. Vectors are applied to gate signals according to predetermined sequences. As a result, the desired voltage waveform is obtained at the output.

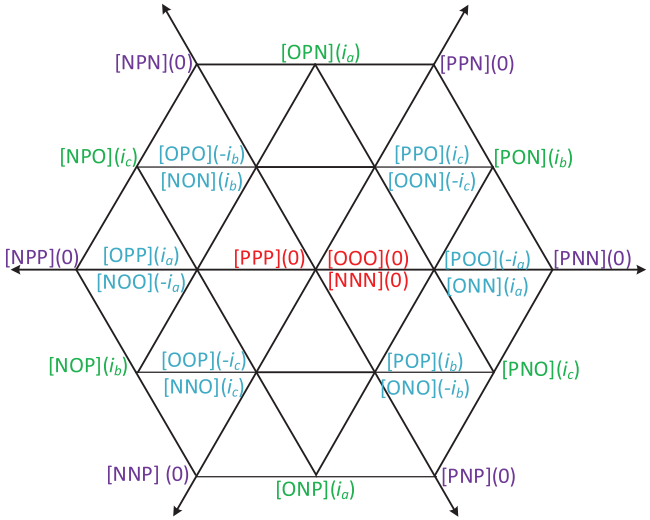

FIGURE 2 Three-level neutral point clamped converter space vector diagram.

The maximum modulation index of the SVPWM method is 15% larger than that of the SPWM method, and similar to the SPWM method, SVPWM method does not apply NPP control.

2.3 | Nearest triangular vector (NTV) modulation

This method is applied as suggested by Pou and his colleagues in [21]. Similar to the SVPWM method, the NTV method uses a space vector diagram to determine the gate signals of the power switches. Different than previous methods, NPP control is performed in the NTV method. After the NPP deviation from the reference value is measured, the neutral point current (i_{np}) direction is controlled to reduce the deviation of the NPP. The phase current equivalent and direction of neutral point current (i_{np}) are shown for every voltage vector in Figure 2. In the figure, small voltage vectors are shown in the colour blue, and there are two alternatives for each small vector. Each of these vectors applies the same neutral point current but in the opposite direction. Therefore, the direction of (i_{np}) can be controlled without affecting the output voltage. The closest three voltage vectors to the equivalent voltage vector are used to

obtain the desired output voltage. The sequence of vectors is predetermined to achieve the minimum number of switches.

The advantage of this method is its ability to limit the NPP ripple. However, the method relies heavily on the small vectors in the space vector diagram. Therefore, having reference vectors far away from the small vectors causes a decrease in its ability to reduce the NPP ripple. Another disadvantage of the method is having a changing number of switchings in each switching period.

2.4 | Symmetric SVWPM method

The symmetric SVPWM method is proposed by Pou et al. [21] to reduce the negative effects of the NTV method. The paper [21] suggested the term step as a measure of the voltage level change for the inverter in a given switching period. If the switch state of a phase changes between P and O or O and N, then this is considered 1 step. If the switch state of a phase changes between P and N, then this is considered as 2 steps. In the NTV method, the total step number of the inverter is either 4 or 8 depending on the operating conditions. On the other hand, the step number is constant at 6 in the symmetric SVPWM method. Due to this property, the symmetric SVPWM method produces better output voltage spectra than the NTV method. However, the low-frequency NPP ripple of this method is larger than the NTV method [21].

2.5 | Equal O-state method

The selected fifth method was first proposed in [19]. The method creates two reference signals for each phase to determine the gate signals of power switches. Given that the neutral point potential has no deviation, reference signals are produced to make all O-state dwell times of phases equal to each other. The method follows four fundamental principles while determining the dwell time of switch states.

- Establishment of the desired line-to-line output voltage at the inverter's output.
- Ensuring equal dwell time for O states across all phases.
- Maintaining a zero dwell time for the N state in the phase with the highest voltage.
- Maintaining a zero dwell time for the P state in the phase with the lowest voltage.

The second principle guarantees the absence of any net current flow to the neutral point current during each switching period. Nevertheless, if there is a deviation in the neutral point potential, the dwell time of O states will be altered by Δd to generate a compensating current. The value of this compensating current, i_{cmp}, is calculated based on the NPP deviation, the DC capacitor values, and the switching period. This correlation is defined in (1). Subsequently, Δd is determined using (2), where i_2 denotes the instantaneous phase current of the phase associated with medium voltage.

$$i_{cmp} = \frac{\Delta v_{np}(C_{top} + C_{bot})}{T_{sw}} \tag{1}$$

$$i_{cmp} = 2(\Delta d) i_2 \tag{2}$$

This method is investigated in this study because of its complete elimination of the low-frequency NPP ripple. However, although the low-frequency NPP ripple is completely eliminated, switching losses are significantly increased in the method [19]. This is an important drawback of the method. In this study, this method is referred to as the equal O-state method to distinguish it from the other methods.

3 | NPP RIPPLE VARIANCE WITH OPERATING PARAMETERS

The NPP ripple contains two components. The first one is the high-frequency or switching-frequency NPP ripple component. The frequency of this ripple type is in the range of the switching frequency of the inverter. Therefore, this ripple type is beyond the control bandwidth of the inverter. The second NPP ripple type is the low-frequency NPP ripple. The frequency of this ripple type is three times the fundamental frequency of the inverter. Therefore, this ripple type is within the control bandwidth of the inverter. The modulation methods with NPP ripple control aim to reduce the low-frequency ripple.

Four main operation parameters affect the low-frequency NPP ripple. These parameters are load current, fundamental frequency, modulation index, and power factor. The low-frequency NPP ripple and load current are directly proportional; that is, when all the other operating parameters are constant, the low-frequency NPP ripple linearly increases with the load current. Moreover, the fundamental frequency and the low-frequency NPP ripple are inversely proportional because the period of the low-frequency NPP ripple is linearly proportional to the fundamental period. However, the effect of the modulation index and the power factor on the low-frequency NPP ripple differs among PWM methods. This section is dedicated to exploring and analysing these differences.

As the first step, a fast model that can be used to calculate the low-frequency NPP ripple is obtained. The model is an extended version of the low-frequency PWM model suggested in [21]. Voltage reference signals and load currents are provided as inputs to the models. Duty cycles of applied voltage vectors are calculated. The neutral point current can be decided since the neutral point current i_{np} is known for every voltage vector as shown in Figure 2. Integrating the neutral point current and dividing the result by two times the DC-link capacitance of the capacitors ($2C$) provides the low-frequency NPP ripple. The main advantage of the model is being able to find the low-frequency NPP ripple without modelling any circuits or circuit elements. On the other hand, high-frequency effects caused by the switching cannot be observed. High-frequency NPP ripple and DC-link ripple are analysed later in Section 5

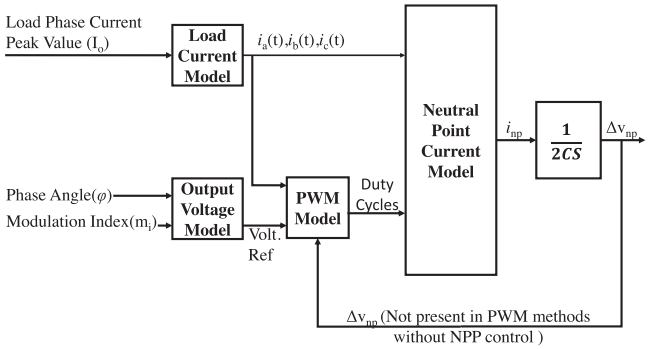

FIGURE 3 Low-frequency neutral point potential ripple model.

using MATLAB Simulink models in which power switches are included.

The block diagram of the low-frequency NPP ripple model is provided in Figure 3. In the figure, voltage ripple is provided back into the PWM model. This feedback is necessary for PWM methods with NPP control. On the other hand, the connection is absent for PWM methods without NPP control. Models are executed in the MATLAB Simulink environment. The input voltage is selected as $V_{\mathrm{DC}} = 800$ V, one input capacitor capacitance is selected as $C = 1$ mF, and the fundamental frequency is selected as $f = 50$ Hz. The results of the low-frequency NPP ripple model are provided for each PWM method in the rest of this section.

3.1 | Low-frequency NPP ripple with SPWM

Among the PWM methods under investigation, SPWM is the only approach for which the NPP ripple can be analytically computed. The derivation is as follows: Voltage reference signals and phase currents are given in (3) and (4), where m_i represents the modulation index, ω represents the electrical angular frequency, and φ represents the power angle. The next expression given in (5) shows the duty cycles for switch position O for the three phases. Conditional statements are eliminated in (6). For one switching period, the neutral point current can be expressed in terms of phase currents and duty cycles of the O states of each phase as given in (7). Combining these expressions, the neutral point current is derived as provided in (8). The derivation includes several trigonometric steps to reach (8). These steps are skipped for the sake of simplicity.

The neutral point current is flowing through two DC-link capacitors. Therefore, the relationship between the neutral point voltage and the neutral point current is shown in (9).

$$\begin{aligned} v_a(t) &= m_i \cos(\omega t) \\ v_b(t) &= m_i \cos\left(\omega t - \frac{2\pi}{3}\right) \\ v_c(t) &= m_i \cos\left(\omega t - \frac{4\pi}{3}\right) \end{aligned} \tag{3}$$

$$\begin{aligned} i_a(t) &= I_o \cos(\omega t - \varphi) \\ i_b(t) &= I_o \cos\left(\omega t - \frac{2\pi}{3} - \varphi\right) \\ i_c(t) &= I_o \cos\left(\omega t - \frac{4\pi}{3} - \varphi\right) \end{aligned} \tag{4}$$

$$\begin{aligned} &if\ v_a(t) > 0 \text{ then } d_{2a} = 1 - m_i \cos(\omega t), \\ &if\ v_a(t) < 0 \text{ then } d_{2a} = 1 + m_i \cos(\omega t), \\ &if\ v_b(t) > 0 \text{ then } d_{2b} = 1 - m_i \cos\left(\omega t - \frac{2\pi}{3}\right), \\ &if\ v_b(t) < 0 \text{ then } d_{2b} = 1 + m_i \cos\left(\omega t - \frac{2\pi}{3}\right), \\ &if\ v_c(t) > 0 \text{ then } d_{2c} = 1 - m_i \cos\left(\omega t - \frac{4\pi}{3}\right), \\ &if\ v_c(t) < 0 \text{ then } d_{2c} = 1 + m_i \cos\left(\omega t - \frac{4\pi}{3}\right) \end{aligned} \tag{5}$$

$$\begin{aligned} d_{0a} &= 1 - m_i |\cos(\omega t)|, \\ d_{0b} &= 1 - m_i \left|\cos\left(\omega t - \frac{2\pi}{3}\right)\right|, \\ d_{0c} &= 1 - m_i \left|\cos\left(\omega t - \frac{4\pi}{3}\right)\right| \end{aligned} \tag{6}$$

$$i_{np}(t) = d_{0a} i_a(t) + d_{0b} i_b(t) + d_{0c} i_c(t) \tag{7}$$

$$\begin{aligned} i_{np}(t) = &- m_i I_o \Big[\left|\cos(\omega t)\right| \cos(\omega t - \varphi) \\ &+ \left|\cos\left(\omega t - \frac{2\pi}{3}\right)\right| \cos\left(\omega t - \varphi - \frac{2\pi}{3}\right) \\ &+ \left|\cos\left(\omega t - \frac{4\pi}{3}\right)\right| \cos\left(\omega t - \varphi - \frac{4\pi}{3}\right) \Big] \end{aligned} \tag{8}$$

$$\Delta V_{\mathrm{NPP}}(t) = \frac{1}{2C} \int i_{np}(t) dt \tag{9}$$

The neutral point current relationship in (8) shows that the neutral point current and the NPP ripple are linearly proportional with load current and modulation index. Low-frequency NPP ripple model results of the SPWM method are provided in Figure 4a. These results show consistency with analytical calculations, where the NPP ripple increases proportionally with the modulation index and decreases as the power factor increases.

3.2 | Low-frequency NPP ripple with SVPWM

Low-frequency NPP ripple model results for SVPWM methods are provided in Figure 4b. The results are different for the low modulation index and the high modulation index regions. This is because different voltage vectors are used in low- and high-modulation index cases.

A low modulation index causes an equivalent voltage vector to be positioned inside the inner hexagon given in Figure 2.

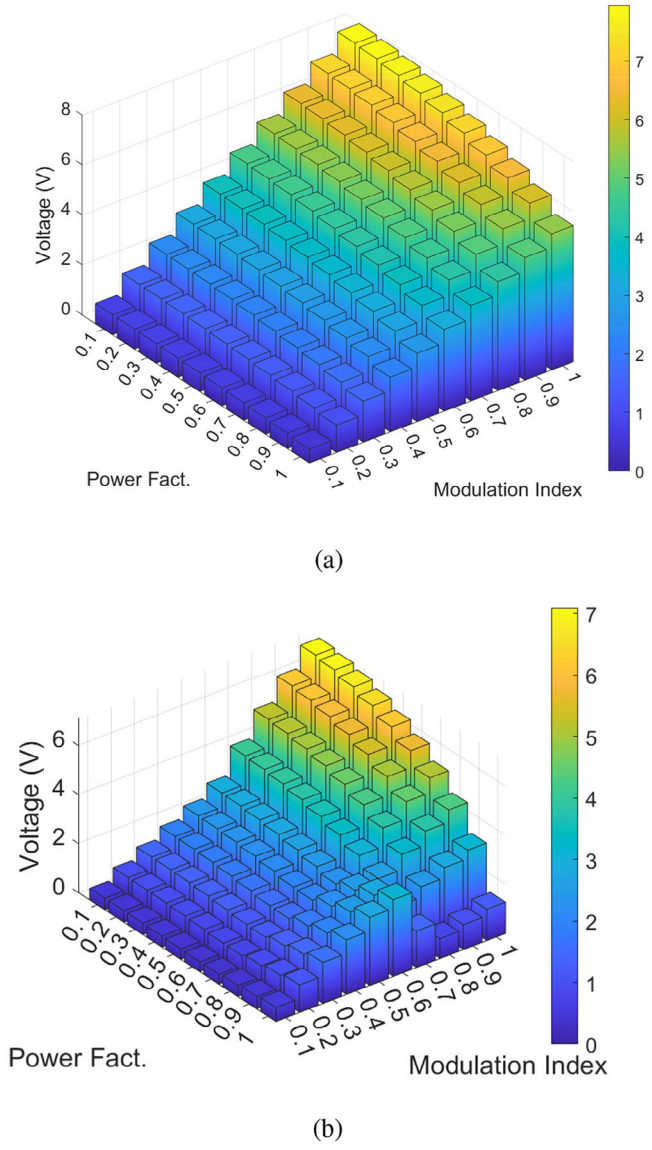

FIGURE 4 Low-frequency neutral point potential (NPP) ripple characteristics of methods with no NPP control. (a) SPWM and (b) SVPWM methods.

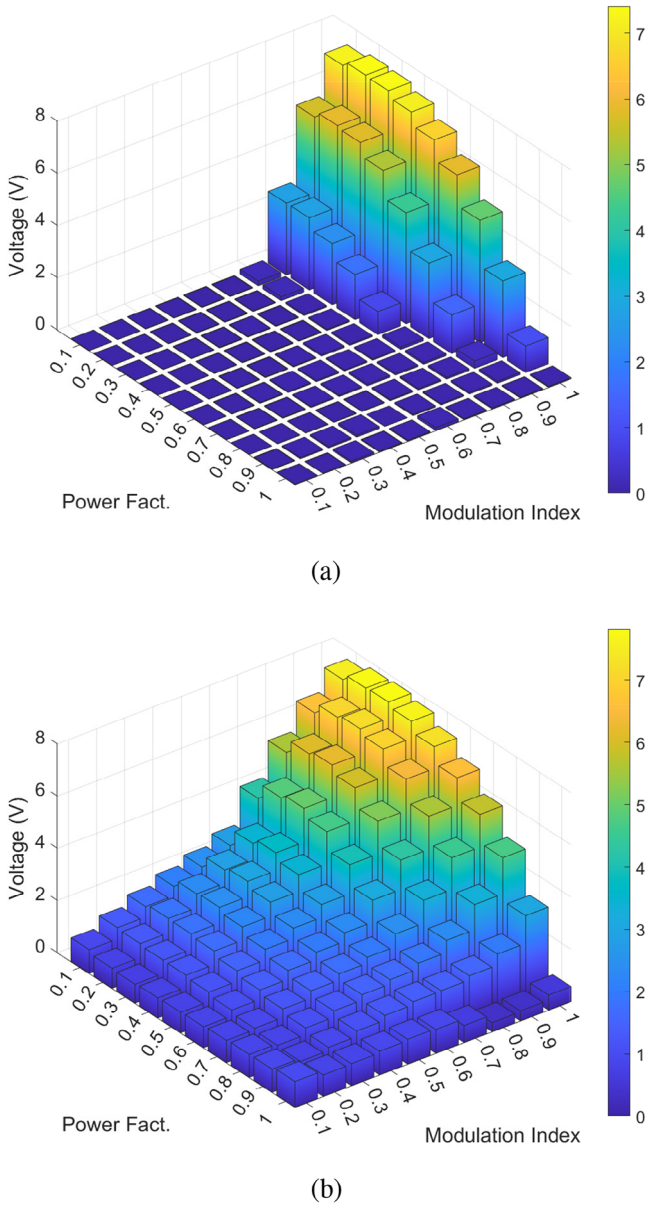

FIGURE 5 Low-frequency neutral point potential (NPP) ripple characteristics of methods with NPP control. (a) Nearest triangle vector and (b) symmetric space vector pulse width modulation methods.

Under these circumstances, only zero vectors and small vectors are used. Zero vectors cause zero neutral point current, while small vectors cause non-zero neutral point current. Since the duty cycle of small vectors increases with increasing modulation index in the inner hexagon region, increasing modulation index increases the low-frequency NPP ripple.

At larger modulation index values, the outer hexagon is used. In this region, small voltage vectors, medium voltage vectors, and large voltage vectors are used. Large voltage vectors cause zero neutral point current, and small vectors mostly cancel the effect of each other on the neutral point current. Hence, medium voltage vectors are the main reason behind the low-frequency NPP ripple. Increasing the modulation index increases the weight of the medium voltage vectors on the duty cycle. As a result, increasing the modulation index increases the low-frequency NPP ripple.

3.3 | Low-frequency NPP ripple with NTV method

The low-frequency NPP ripple result of the NTV method that is shown in Figure 5a is consistent with the literature [21]. For operating points with a low modulation index and/or high power factor, the low-frequency NPP ripple is zero. At the inner hexagon of the space vector diagram, the NPP ripple is eliminated because only small vectors and zero vectors are used in this region. Since zero vectors cause zero neutral point current and the direction of neutral point current can be controlled with small vector selection, it is possible to obtain zero average neutral point current for every switching period in the inner hexagon. However, for operating points with a large

modulation index and low power factor, NPP ripple is non-zero. At the larger hexagon, the neutral point current occurs because of medium voltage vectors and small voltage vectors. The direction of the neutral point current can not be controlled while applying medium voltage vectors since there is only one possible vector. Therefore, the direction of the neutral point current should be controlled with small vectors to compensate for the effect of medium voltage vectors. As the modulation index increases, the weight of medium voltage vectors on the duty cycle increases; therefore, the low-frequency NPP ripple increases.

3.4 | Low-frequency NPP ripple with symmetric SVPWM

The low-frequency NPP ripple behaviour of the symmetric SVPWM method that is shown in Figure 5b is similar to the NTV method. However, while only three different voltage vectors are used in every switching period in the NTV method, four vectors are used in the symmetric SVPWM method. This adds a new constraint to NPP ripple control; therefore, its NPP ripple reduction performance is limited compared to the NTV method.

3.5 | Low-frequency NPP ripple with the equal O-state method

The equal O-state method can provide zero low-frequency NPP ripple on all operating points. This fact is based on several principles. The duration time of O-state of each phase can be made equal to each other. Since the summation of phase currents is equal for any instantaneous time, the average neutral point current (i_{np}) can be zero for each switching period. If there is a deviation from zero volts in NPP, then the duration of O-states is modified to reduce the NPP deviation. The equal O-state method is tested with the low-frequency NPP ripple model and no low-frequency NPP ripple is observed. Therefore, its low-frequency NPP ripple characteristics are not shown in Figures 4 and 5.

To summarize, the results suggest that four PWM methods, SPWM, SVPWM, NTV method, and symmetric SVPWM—have the highest low-frequency NPP ripple at high modulation index and low power factor regions. On the other hand, for the equal O-state method, the modulation index and the power factor are ineffective for low-frequency NPP ripple.

4 | MOTOR DRIVE APPLICATION

NPP ripple is affected by the operating conditions of an inverter, as shown in previous sections. Therefore, the NPP ripple is application-dependent. A reference motor with a power rating of 100 kW is selected to observe the NPP ripple on the operating conditions of a motor drive application.

TABLE 1 Parameters of ten selected operating points.

OP No.	f_{fund} (Hz)	Phase current (A)	Power factor
1	3	184.3	0.81
2	33	182.9	0.81
3	70	182.3	0.74
4	100	182.9	0.74
5	130	183.8	0.75
6	140	177.3	0.77
7	173	162.8	0.80
8	210	144.8	0.82
9	273	125.9	0.82
10	400	81.3	0.88

The electric motor under investigation is a permanent magnet-assisted synchronous reluctance machine (PMaSynRM) with ferrite permanent magnets. This machine type was selected due to the rising interest in its usage in traction applications. According to [8], the absence of rare-earth permanent magnets makes synchronous reluctance machines favourable. However, PMaSynRM may exhibit lower power factor values and a lower pole count compared to interior permanent magnet synchronous machines (IPMSMs), necessitating the use of a higher DC-link capacitor.

NPP ripple depends on load current, frequency, power factor, and modulation index. Therefore, it is important to understand how these parameters are affected by the speed and torque of the motor. The motor characteristic maps shown in Figure 6, illustrate these relationships. To determine the capacitor size, it is crucial to identify the operating point with the highest NPP ripple. As discussed in Section 3, potential operating points with the highest NPP ripple are determined, considering high load current, high modulation index, low power factor, and low fundamental frequency regions. A total of ten points are selected and marked in Figure 6d, and their operating parameters are listed in Table 1. Selecting a capacitor based on these points ensures limited low-frequency NPP ripple in all motor operating regions.

5 | CAPACITOR SIZING

In this section, the DC-link capacitance value is determined for each of the five different PWM methods. To determine the capacitor sizes, distinct models are implemented in the MATLAB Simulink environment for each PWM method. It is essential to note that the switching effects, and thus the high-frequency ripples, are included in these models. The 3L-NPC inverter topology is employed in these models, with a switching frequency of 50 kHz. This specific frequency is selected to minimize the high-frequency NPP ripple, allowing for a more focused analysis of the low-frequency NPP ripple. Low-frequency NPP ripple is focussed because this type of ripple serves as the primary limiting factor for determining the DC-link capacitor size in most PWM methods.

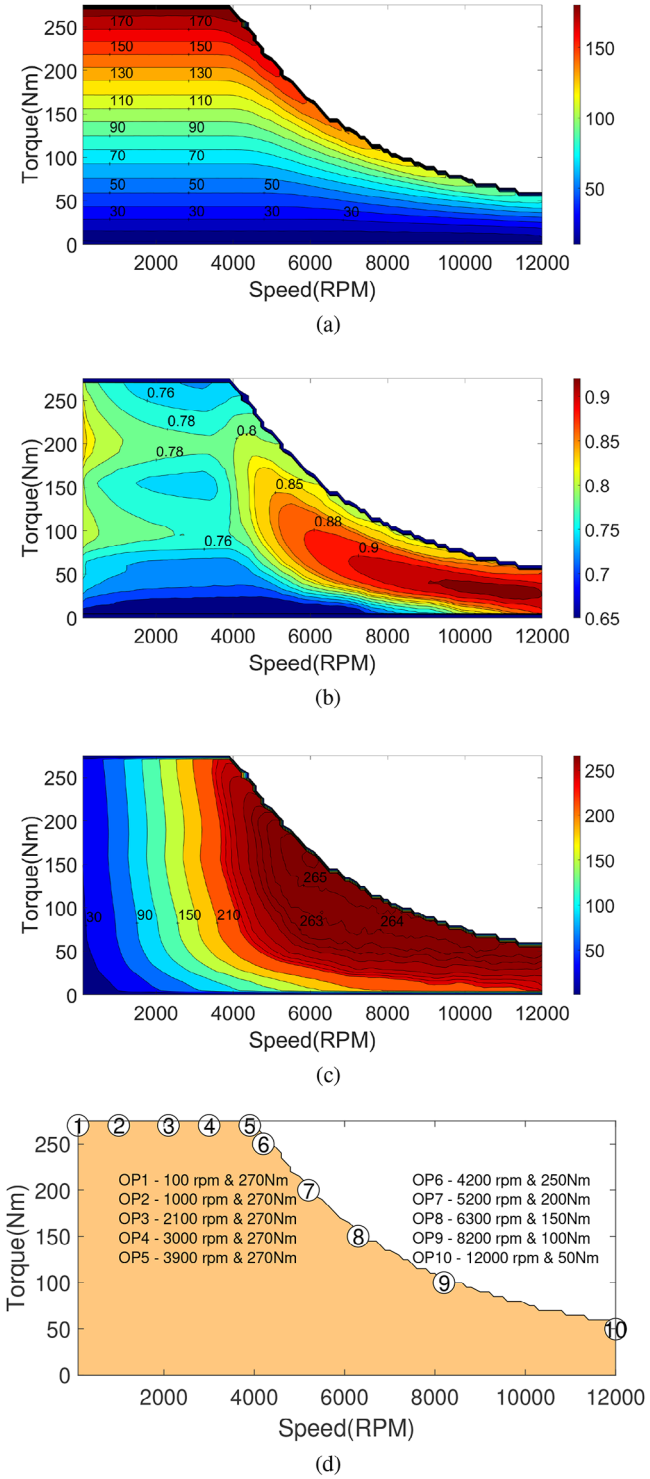

FIGURE 6 Motor characteristic maps and selected operating points. (a) Motor characteristic current map. (b) Motor characteristic power factor map. (c) Motor characteristic voltage map and (d) selected operating points (OPs).

Two types of voltage ripples are calculated. The first one is the NPP ripple, which is defined as the voltage ripple on the bottom capacitor (C_B) voltage. The other ripple is the DC-link voltage ripple. This ripple is defined as the ripple on the combined voltage (V_{DC}) of the top capacitor and the bottom capacitor. Hence, if both of these ripples are below the desired level, then the capacitor size requirement is satisfied.

The input voltage is applied as 800 V_{DC}. The input DC voltage source is considered a battery and modelled with an ideal voltage source. Line impedance is applied as zero and the load is modelled as an RL load. The top and bottom currents of the inverter, i_{top} and i_{bot} are measured as shown in Figure 1. Measured current i_{top} has two components: DC component and AC component. The DC voltage source connected to the input of the inverter is assumed to be providing only DC current. As a result, due to Kirchhoff's current law, the AC component of i_{top} flows through C_{top}. In this case, AC voltage on C_{top} can be calculated by integrating the AC component of i_{top} and dividing it by C_{top}. Using the same method with C_{bot} and i_{bot}, AC voltage on C_{bot} can be calculated. The difference between the maximum and minimum peak of AC voltage on C_{bot} is considered as the NPP ripple. To find DC-link voltage ripple, AC voltage on C_{top} and AC voltage on C_{bot} are summed, and the difference between the maximum and minimum peak of the resulting signal is considered as DC-link voltage ripple. This calculation process is summarized as follows:

$$
\begin{aligned}
i_{top} &= i_{top(AC)} + i_{top(DC)} \\
i_{bot} &= i_{bot(AC)} + i_{bot(DC)} \\
V_{top(AC)} &= \frac{1}{C_{top}} \int i_{top(AC)}\, dt \\
V_{bot(AC)} &= \frac{1}{C_{bot}} \int i_{bot(AC)}\, dt \\
V_{DC\text{-}link(AC)} &= V_{top(AC)} + V_{top(DC)}
\end{aligned}
\tag{10}
$$

First, DC link sizing results are given in the following two subsections. Sizing for the first four methods (SPWM, SVPWM, NTV and symmetric NTV) is carried out considering low-frequency NPP ripple only. Then, high-frequency ripple components both at NPP and DC-link are considered for the equal O-state method.

5.1 | Sizing for SPWM, SVPWM, NTV and symmetric NTV methods

As the first step, the simulation models are run on all ten operating points identified in Section 4. Simulation results for OP4 (operating point with 3000 rpm and 270 Nm) are presented in Figures 7–11. In these results, waveforms of line-to-line voltage V_{ab}, three phase currents i_a, i_b, i_c and the neutral point voltage V_{np} are shown. The results verify that the PWM methods are modelled successfully.

Furthermore, the effect of line inductance between the DC source and DC-link capacitors on NPP ripple is investigated. For this purpose, the NPP ripple is measured with two different methods. The first one has already been explained before. The other method is measuring the voltage of C_B and identifying the peak-to-peak difference. In the first method, the current

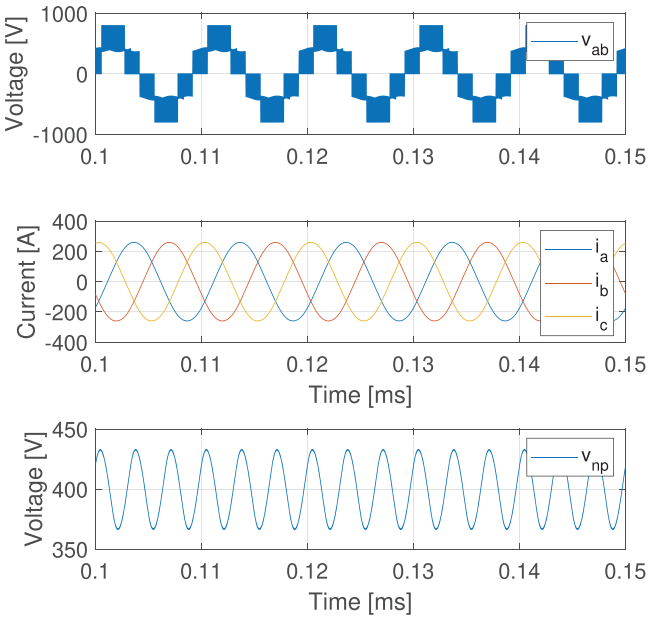

FIGURE 7 Simulation results with sinusoidal pulse width modulation for OP4 with $C = 1000$ μF.

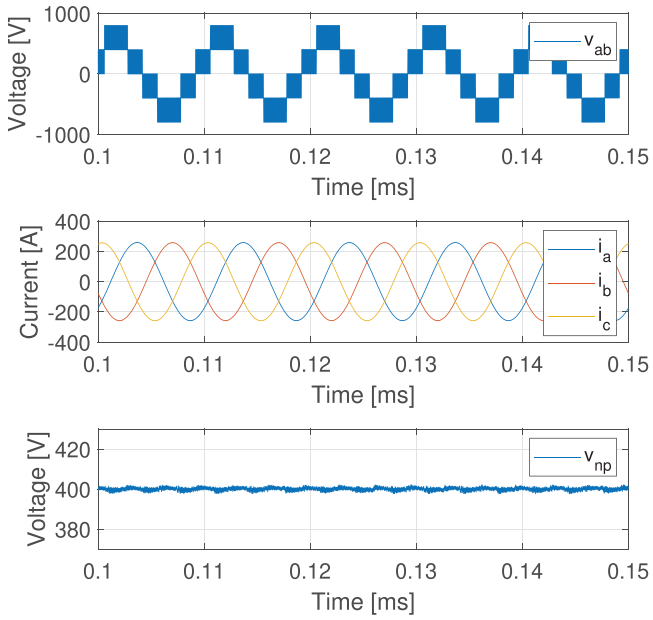

FIGURE 9 Simulation results with the nearest triangle vector for OP4 with $C = 1000$ μF.

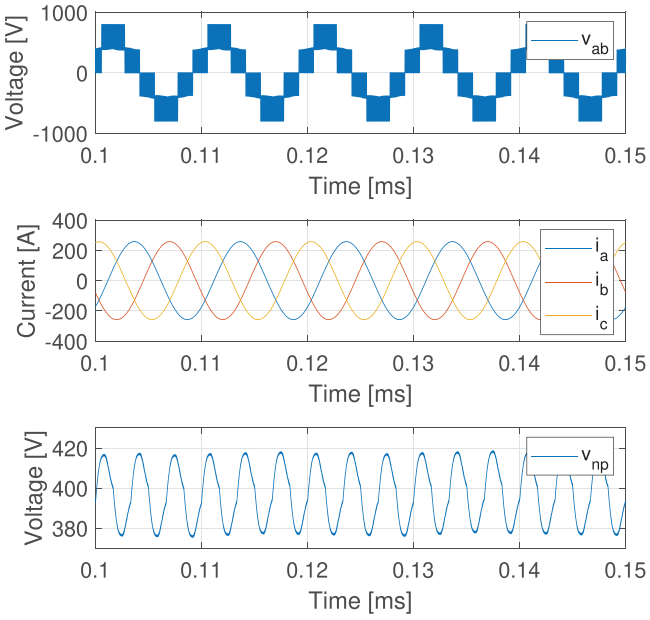

FIGURE 8 Simulation results with space vector pulse width modulation for OP4 with $C = 1000$ μF.

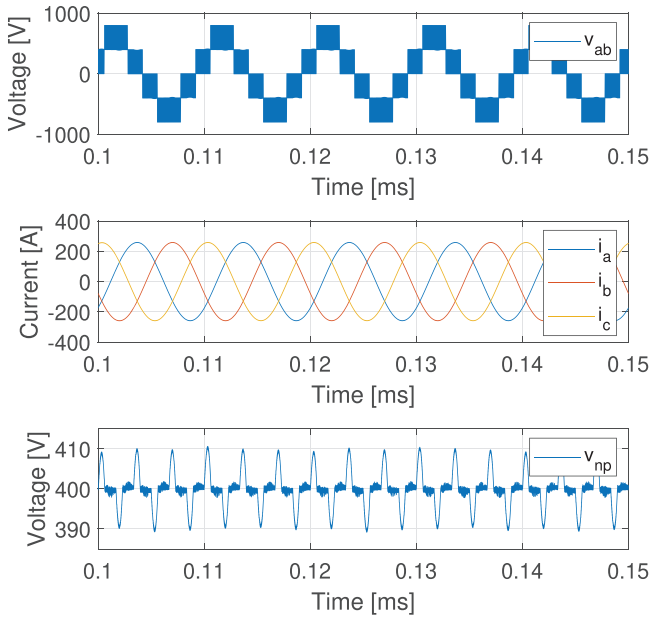

FIGURE 10 Simulation results with symmetric space vector pulse width modulation for OP4 with $C = 1000$ μF.

flowing from the DC voltage source to the DC-link capacitors is assumed to be constant DC. However, in the second method, the DC voltage source provides a non-constant current and therefore, has an AC component. Hence, the line impedance between the DC voltage source and the DC-link capacitor is assumed to be infinite in the first method and it is assumed to be zero in the second method.

NPP ripple is measured for ten selected operating points and the results are presented in Figure 12. The ripple is not measured for the equal O-state method since this method already has zero NPP ripple. In the results, OP1 has the highest NPP ripple due to its low motor speed and related low fundamental electrical frequency. This is an expected result because of the inverse relationship between inverter frequency and the low-frequency NPP ripple. Moreover, the high line impedance results and the zero impedance results are close to each other for operating points number 2 or higher. Therefore, the effect of line impedance is found to be insignificant except for very low-speed operating points.

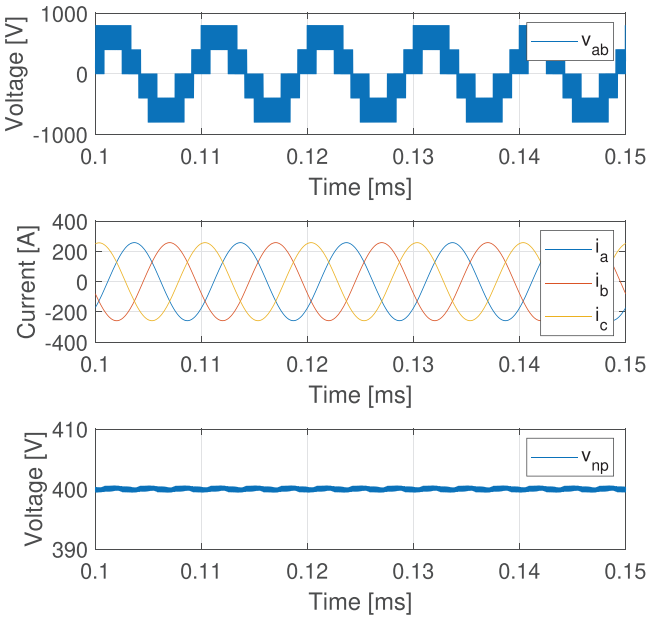

FIGURE 11 Simulation results with the equal O-state method for OP4 with $C = 1000$ μF.

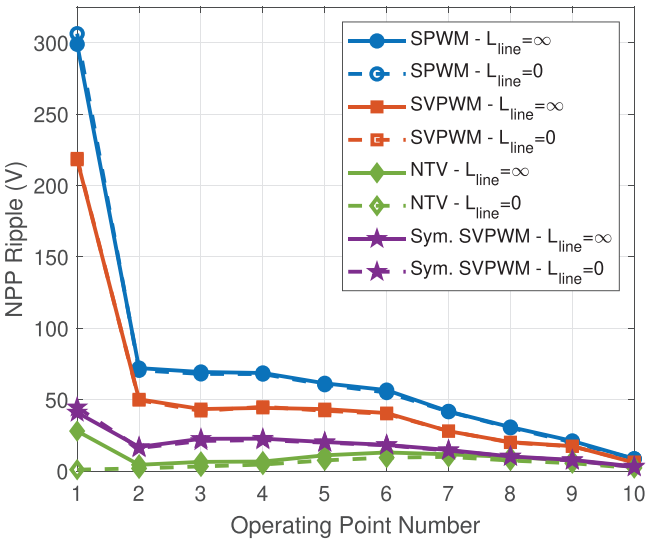

FIGURE 12 Neutral point potential peak–peak ripple at selected operating points with $C = 1000$ μF.

In addition to NPP ripple, DC-link voltage ripple is investigated using the models. The measurement is implemented as presented in (10). So it is assumed that the DC voltage source can only provide DC constant current. The results are presented in Figure 13 for SPWM, SVPWM, NTV, and symmetric SVPWM methods. The high DC-link ripple at OP1 corresponds to a 3.33 Hz fundamental frequency. Since this is a low-frequency AC signal, this signal can be regulated by the battery in a real system.

The results suggest that NPP ripple is higher than DC-link ripple for four PWM methods. Thus, for SPWM, SVPWM,

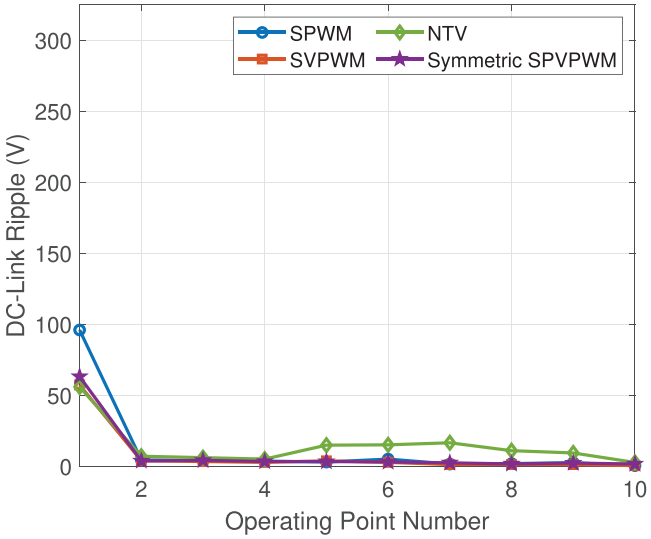

FIGURE 13 DC-link peak–peak ripple at selected operating points with $C = 1000$ μF.

NTV, and symmetric SVPWM methods, the NPP ripple is the limiting factor. Therefore, capacitor sizing should be performed concerning the NPP ripple value. However, in the equal O-state method, NPP ripple and total DC-link voltage ripple must both be considered while sizing the DC-link capacitors.

It is important to point out that, NPP ripple values of the SPWM and SVPWM methods are unbounded as the frequency approaches zero, and thus it is not possible to select a worst-case operating point. This shows that if a modulation with no NPP control is applied, the allowed operation region of the drive system must be restricted in the low-speed and high-torque region. Most importantly, it is evident that a reliable modulation method with NPP control is a must in a high-performance drive system. By assuming that low speed and high torque operation regions are limited in SPWM and SVPWM methods, OP2 (1000 rpm) is chosen as their worst operating point. NTV OP6 (4200 rpm) and symmetric SVPWM OP4 (3000 rpm) are selected as the worst OPs. At the selected worst operating points, the capacitor size needed to keep the NPP ripple under the desired limit is calculated with the inverse proportion given in (11). The resulting worst cases and required capacitor sizes are listed in Table 2 for 5%, that is 40 V peak-to-peak NPP ripple, 10% that is 80 V peak-to-peak NPP ripple and 12.5% that is 100 V peak-to-peak NPP ripple values.

$$C_{\text{ini}}\Delta V_{\text{NPP(worst-case)}} = C_{\text{final}}\Delta V_{\text{NPP(limit)}} \tag{11}$$

5.2 | Sizing for equal O-state method

For the equal O-state method, candidate operating points are invalid since low-frequency NPP ripple is zero for all operating points. Therefore, voltage ripple caused by switching effects is investigated in the whole motor operating region. The motor operating region is represented by 60 operating points with varying torque and speed values. The simulations are executed

TABLE 2 Worst OPs and required capacitance for each DC-link capacitor.

PWM method	Worst OP	Ripple limit	Capacitance
SPWM	#2	5%	1900 μF
SPWM	#2	10%	950 μF
SPWM	#2	12.50%	760 μF
SVPWM	#2	5%	1200 μF
SVPWM	#2	10%	600 μF
SVPWM	#2	12.50%	480 μF
NTV	#6	5%	325 μF
NTV	#6	10%	160 μF
NTV	#6	12.50%	130 μF
Symmetric SVPWM	#4	5%	550 μF
Symmetric SVPWM	#4	10%	275 μF
Symmetric SVPWM	#4	12.50%	220 μF

Abbreviations: NTV, nearest triangle vector; OP, operating point; PWM, pulse width modulation; SPWM, sinusoidal PWM; SVPWM, space vector PWM.

for all 60 operating points. Both the DC-link voltage ripple and the NPP ripple are observed. Similar to previous models, two current measurements ($i_{top}(t)$ and $i_{bot}(t)$) are used to obtain peak-to-peak NPP ripple and DC-link potential ripple.

The inverse relationship between the voltage ripple and capacitor size cannot be used for the equal O-state method. Thus, an initial value for the DC-link capacitance is selected as 10 μF and once the NPP ripple and DC-link ripple are determined, the capacitor size is progressively increased until both the NPP ripple and the DC-link ripple are below the specified ripple limit. The highest DC-link voltage ripple and the NPP ripple are observed when the torque is 270 Nm and the speed is 400 rpm. The required capacitance for one of the DC-link capacitances is found to be 220 μF for 5% ripple restriction.

To sum up, the results suggest that different PWM methods have different worst operating conditions in terms of NPP ripple. However, all five PWM methods have the worst operating points on high-load current regions, corresponding to high torque regions. This is an expected result since the low-frequency NPP ripple is proportional to the load current. The worst operating point of SPWM and SVPWM methods is OP2 because of the low motor speed and, therefore, low fundamental frequency. On the other hand, the NTV method can suppress low-frequency NPP ripple at low modulation indexes as observed in Figure 5a. As a result, different from the SPWM and SVPWM methods, the NTV method has the worst operating point in the high modulation index region. Symmetric SVPWM can not completely suppress NPP ripple in the low modulation index region. As a result, symmetric SVPWM has the worst OP in OP4. The equal O-state PWM method has zero low-frequency NPP ripple; therefore, the high-frequency ripple of the DC-link voltage and NPP ripple are determining factors of the capacitor size. Since high-frequency NPP ripple depends on the load current, DC-link and NPP ripples are highest in a high torque region.

The equal O-state method is found to have the lowest DC-link capacitance. This is an expected result since this method can suppress NPP ripple better than other methods.

6 | LOW-SPEED OPERATION FOR SPWM AND SVPWM METHODS

As mentioned in Section 5, NPP ripple dramatically increases under low-speed operating conditions for SPWM and SVPWM methods. In this section, a possible solution to this problem is proposed. A large ripple at the neutral point forms because of the neutral point current. Considering Figure 2, the neutral point current is non-zero for small-size vectors and medium-size vectors. Therefore, applying zero dwell time for small-size vectors and medium-size vectors results in zero neutral point current and consequently zero NPP ripple.

Every voltage vector required to operate the SPWM or SVPWM method can be expressed as a vector summation of six large vectors and zero vectors. Therefore, all the operating points required to run the motor can be applied to the inverter by using large vectors and zero vectors. Effectively, the inverter would act as a 2L-VSI. The output voltage will have two levels. The calculation of dwell times for vectors is the same as the two-level SVPWM method.

Using only large vectors and zero vectors to operate a 3L-NPC VSI would effectively be a new PWM method. This PWM method is named the large vector PWM method in this paper. The method is proposed to offer a solution for the low-speed operation problem of the SPWM and SVPWM methods. In this solution, while applying SPWM and SVPWM to a motor drive inverter, the PWM method switches to a large vector PWM under a predetermined motor speed. As a result, large NPP ripples at the neutral point can be avoided.

7 | MODIFIED MOTOR CASE STUDIES

In 3L-NPC inverter operation, frequency and power factor have important effects on the NPP ripple magnitude, as shown in Section 3. Hence, designing traction motors having different power factor values and fundamental frequency ratings can change the size of the DC-link capacitor. To identify the magnitude of the capacitor change, different motor designs are simulated and analysed in this section by modifying the motor's power factor and fundamental frequency.

7.1 | High power factor motor case

As shown in Section 3, all PWM methods except for the equal O-state method provide a decrease in the NPP ripple in cases of increasing power factor. In the NTV case, power factor improvement does not provide a lower NPP ripple at low modulation indexes because the NPP ripple is already zero in this

TABLE 3 Capacitor sizing results for the modified motor with power factor of 0.9.

PWM method	Capacitor size initial motor	Capacitor size modified motor	New worst operating condition
NTV	325 μF	225 μF	5
Symmetric SVPWM	550 μF	275 μF	3

Abbreviations: NTV, nearest triangle vector; PWM, pulse width modulation; SVPWM, space vector PWM.

TABLE 4 Capacitor sizing results for the modified motor with double pole pair number.

PWM method	Capacitor size initial motor	Capacitor size modified motor	New worst operating condition
NTV	325 μF	250 μF	7
Symmetric SVPWM	550 μF	310 μF	4

Abbreviations: NTV, nearest triangle vector; PWM, pulse width modulation; SVPWM, space vector PWM.

case. However, at higher modulation indexes, increasing the power factor causes a decrease in the NPP ripple.

Specifically, for the selected drive system, the worst OP for NPP ripple is determined at OP6 in Table 1. Therefore, this point is the limiting factor for the capacitor size. At this point, the power factor is shown as 0.77. Consequently, enhancing the power factor at this operating point can result in a reduced demand for capacitor size. Similarly, the same effect can be observed for the symmetric SVPWM method.

The motor selected for this study is a permanent magnet-assisted synchronous reluctance machine. To increase the power factor of the design, another motor type with a higher power factor, such as an interior permanent magnet synchronous motor, can be selected.

To test the capacitor size change, a change in the motor type is assumed, and the power factor is increased. The same capacitor selection algorithm provided in Section 5 is used again to make a new capacitor selection for the modified motor. In this new motor, the same operating points given in Table 1 are used except for the power factor. The power factor is modified to be 0.90 for each operation point.

The results of the new capacitor size are provided in Table 3. According to the results, capacitor size is reduced by more than 30% for the NTV case and by more than 50% for the symmetric SVPWM case. Therefore, it is verified that an increase in the power factor can provide a significant reduction in the DC-link capacitor size.

7.2 | High-frequency motor case

Another way to reduce the DC-link capacitor size is to increase the fundamental frequency of the traction motor. This is possible by increasing the pole pair number of the motor. For the analysis, it is assumed that the pole number is doubled without changing the other operational parameters given in Table 1. Similar to the previous case, the capacitor selection algorithm given in Section 5 is used. The results of the capacitor selection under these new operating conditions are given in Table 4.

The results show that by doubling the frequency, it is possible to reduce the size of the capacitor by more than 23% and more than 43% in the NTV and symmetric SVPWM methods, respectively.

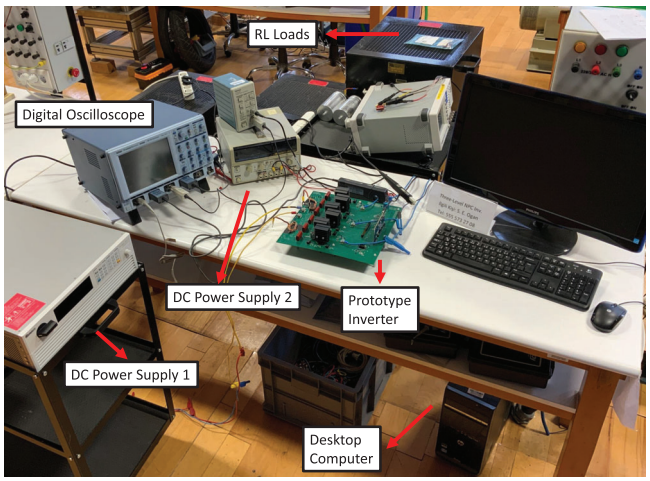

FIGURE 14 Experimental setup.

8 | EXPERIMENTAL VERIFICATION

Experiments are conducted to verify the simulation results with PWM methods. The experimental setup shown in Figure 14 is a scaled version of the motor drive system introduced in Section 4. The 3L-NPC inverter topology is designed on a printed circuit board. The design includes 12 silicon MOSFETs and 6 silicon carbide (SiC) power diodes. To run the control algorithms, feedback is obtained from phase currents and neutral point voltage. These signals are fed back to the control algorithm. Digital signal processor (DSP) TMS320F28379D is used as the digital control unit of the inverter; all the algorithms are run on the DSP and the power switches are controlled accordingly. The switching frequency is selected as 50 kHz. The input voltage is supplied from a constant DC supply, and it is applied at 380 V. DC-link capacitor values are selected at 4.4 μF each. Inductor and resistor banks are used as varying loads at the output. By changing the connected inductor and resistor numbers, varying power factors and impedance values are obtained.

The three of the analysed methods that are SPWM, SVPWM, and the equal O-state methods are experimentally tested. NTV and Symmetric SVPWM methods are not tested as these methods get affected by the noise on the NPP voltage measurement and the measurements on a small-scale setup are not reliable. Four new measurement points are selected based on the

TABLE 5 Experimental results.

Measurement point (MP) no.	PWM method	Peak current	Pf	Mi	Freq.	Capacitance	NPP ripple simulation	NPP ripple experiment
MP1	SPWM	1.95 A	0.76	0.28	33.3 Hz	4.4 μF	84 V	92 V
	SVPWM	1.95 A	0.76	0.28	33.3 Hz	4.4 μF	41 V	65 V
	Equal O-state meth.	1.95 A	0.76	0.28	33.3 Hz	4.4 μF	<2 V	10 V
MP2	SPWM	2.20 A	0.75	0.88	130 Hz	4.4 μF	114 V	94 V
	SVPWM	2.20 A	0.75	0.88	130 Hz	4.4 μF	74 V	62 V
	Equal O-state meth.	2.20 A	0.75	0.88	130 Hz	4.4 μF	<2 V	14 V
MP3	SPWM	1.85 A	0.81	0.94	190 Hz	4.4 μF	70 V	60 V
	SVPWM	1.85 A	0.81	0.94	190 Hz	4.4 μF	44 V	40 V
	Equal O-state meth.	1.85 A	0.81	0.94	190 Hz	4.4 μF	<2 V	14 V
MP4	SPWM	1.00 A	0.88	0.93	400 Hz	4.4 μF	17 V	14 V
	SVPWM	1.00 A	0.88	0.93	400 Hz	4.4 μF	11 V	10 V
	Equal O-state meth.	1.00 A	0.88	0.93	400 Hz	4.4 μF	<2 V	5 V

Abbreviations: NPP, neutral point potential; PWM, pulse width modulation; SPWM, sinusoidal PWM; SVPWM, space vector PWM.

previous findings and are given in Table 5. Furthermore, the simulation results for the four new cases are presented in the same table.

Results verify that the SPWM method has the largest NPP ripple among the three PWM methods, while the equal O-state method has the smallest. Measurement points 1 and 2 have a higher NPP ripple compared to 3 or 4. This is because of the high load current and lower power factor. These two points represent the high torque region in a motor drive application due to the high load current. The experimental NPP results are consistent with the simulation model results as given in Table 5. The difference can be explained by the tolerances of DC-link capacitors, RL loads, stray inductances, and capacitors.

Line-to-line voltage V_{ab}, phase current, and NPP V_{np} waveforms of three PWM methods are recorded and shown in Figures 15–20 for operating point 2. Line-to-line voltage and phase currents are measured simultaneously. On the other hand, NPP is measured separately and thus given as a separate plot. It is verified that NPP ripple in the SPWM and SVPWM methods is sinusoidal, and NPP ripple in the equal O-state method is non-sinusoidal. In the SPWM and SVPWM cases, the low-frequency NPP ripple was the dominant part of the NPP ripple. In the equal O-state method model, the high-frequency NPP ripple part was the dominant part of the NPP ripple. In the NPP waveform, the high-frequency NPP ripple is larger than the simulation results. This is because of several reasons. Interaction between the self-inductance of copper tracks plus MOSFET pins and the output capacitors of MOSFETs causes a ringing effect on the waveform. Moreover, the three-phase RL loads are not ideal. Therefore, they have a slight imbalance and have a changing inductance with frequency; at high frequencies, the effective inductance of the RL load decreases. Therefore, the high-frequency part of the output voltage waveform causes higher spikes in the output current.

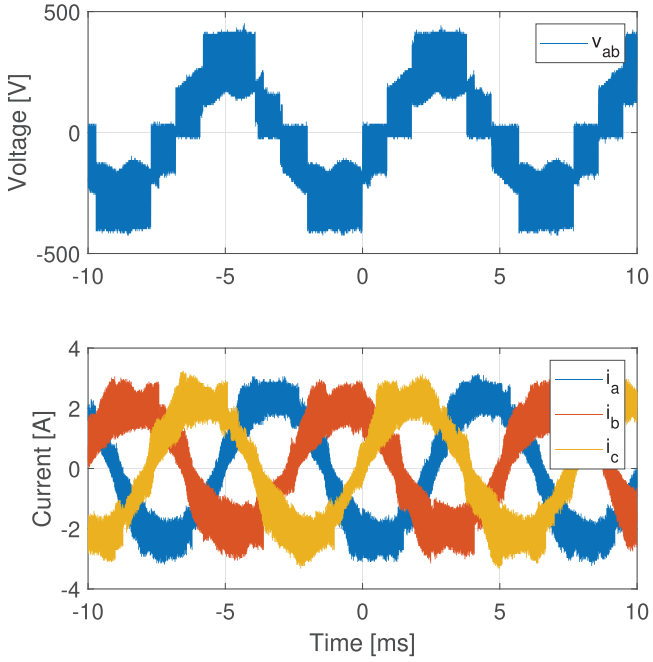

FIGURE 15 Measured line–line voltage and phase currents with sinusoidal pulse width modulation for measurement point 2.

9 | TWO-LEVEL INVERTER CAPACITOR SIZE

As the two-level voltage source inverter is the most common inverter topology in electric vehicle traction applications, this study involves a comparative analysis between the capacitor sizes of a two-level inverter and a 3L-NPC inverter.

Similar to 3L-NPC VSI, the DC-link voltage ripple is determined using a MATLAB Simulink model. The main specifications of the model are listed in Table 6. Current flowing

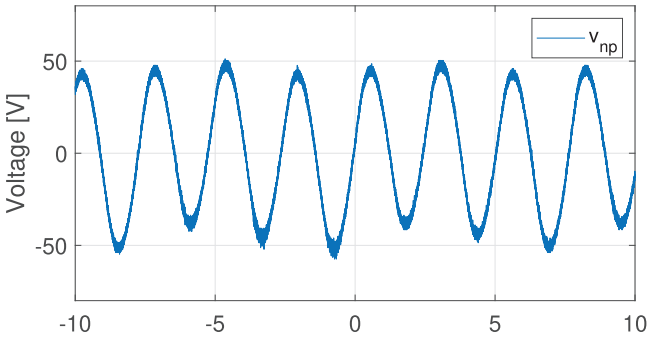

FIGURE 16 Measured neutral point potential with sinusoidal pulse width modulation for measurement point 2.

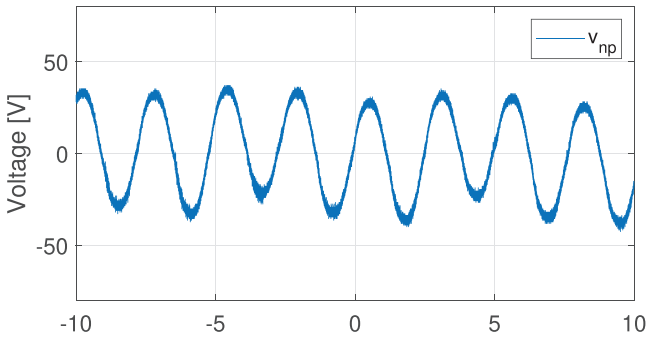

FIGURE 18 Measured neutral point potential with space vector pulse width modulation for measurement point 2.

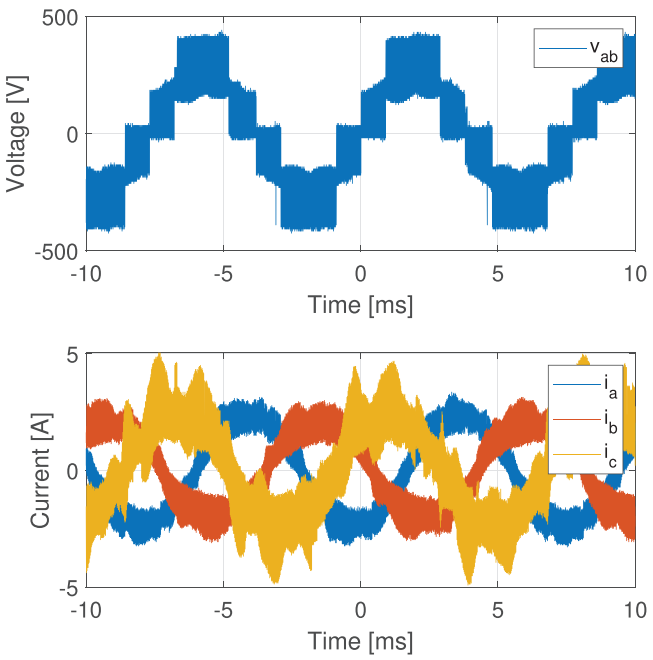

FIGURE 17 Measured line-line voltage and phase currents with space vector pulse width modulation for measurement point 2.

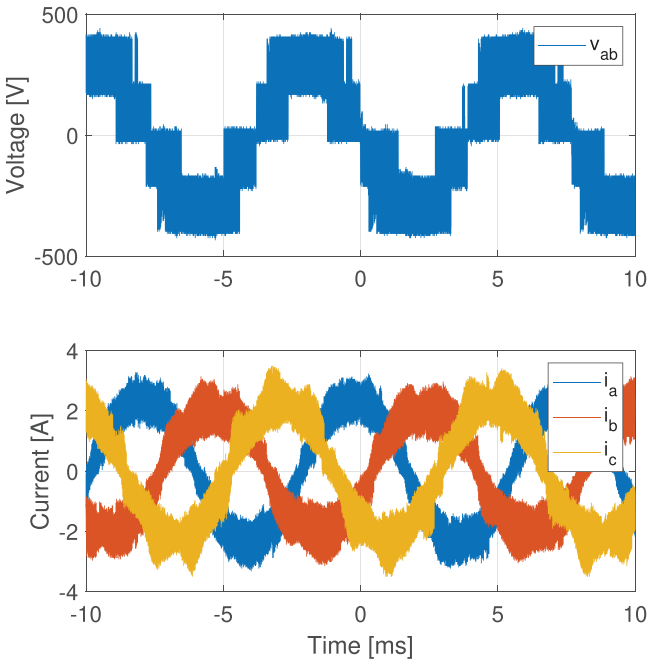

FIGURE 19 Measured line-line voltage and phase currents with equal O-state method for measurement point 2.

TABLE 6 Two-level VSI simulation specifications.

PWM method	SVPWM
Switching frequency, f_{SW}	50 kHz
Load type	RL load
Deadband	1 ms
DC link voltage, V_{DC}	800 V

Abbreviations: PWM, pulse width modulation; SVPWM, space vector PWM; VSI, voltage source inverter.

from the capacitor to the inverter half-bridges is named as i_{top} similar to the 3L-NPC VSI case explained in Section 5. The AC component of i_{top} is integrated to obtain the AC voltage on the DC-link capacitor. The difference between the maximum peak and the minimum peak of this signal is referred to as the DC-link voltage ripple.

The capacitor size is determined to keep the DC-link voltage ripple under 5% for all operating points of the motor. The same operating points used for the equal O-state method are used for this analysis. An initial capacitance value of 100 μF is used and the DC-link voltage ripple is found for all operating points. At the worst operating point, the inverse proportion between the DC-link ripple and the capacitor size is used to obtain the required capacitance size. The inverse proportional relationship used is provided in (12).

$$C_{\text{initial}}\Delta V_{\text{DC(worst-case)}} = C_{\text{final}}\Delta V_{\text{DC(desired)}} \tag{12}$$

The operating point with the highest DC-link voltage ripple is identified to be at $T = 270$ Nm load torque, $n = 400$ rpm motor speed, $m_i = 0.17$ modulation index, 183 A_{rms} load current, and $pf = 0.79$ power factor. Maximum DC-link potential ripple is limited to 5% of the DC-link voltage, which corresponds to 40 V. Under these circumstances, the capacitor size is

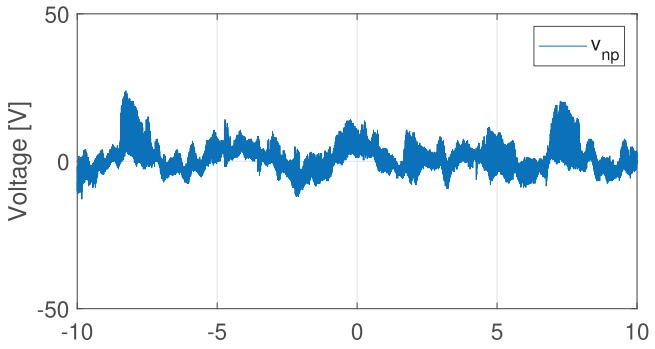

FIGURE 20 Measured neutral point potential with equal O-state method for measurement point 2.

determined as $C = 130\ \mu F$. Furthermore, it is essential to mention that this is going to be the sole DC-link capacitance with a voltage rating higher than 800 V.

In this study, a relatively high switching frequency is applied to be able to distinguish the low-frequency and high-frequency NPP ripples in the 3L-VSI. However, in a 2L-VSI, the main source of the DC-link ripple is the switching [22]. If a switching frequency of around 10–12 kHz was selected, a higher capacitance for the 2L-VSI would be obtained.

10 | DISCUSSION AND CONCLUSION

This study focused on the NPP ripple since it is a dominant effect for 3L-NPC inverter capacitor size. It has been found that the design properties of the motor can be modified to have a smaller DC-link capacitor. In the paper, the investigated motor is modified to double its frequency. As a result, the required DC-link capacitor size is reduced by 23%. Moreover, the investigated motor is modified to have a minimum power factor of 0.9. In this case, the required capacitor size is reduced by 30%. These results provide proof that modifying the motor properties can be used to reduce the capacitor size of the 3L-NPC inverter.

The paper points out an important drawback of 3L-NPC inverter driven with SPWM or SVPWM methods in Section 5. Since the neutral point of the 3L-NPC inverter is floating and not connected to the battery or the DC voltage source, the NPP ripple goes to extremely high values when the motor speed is low. This is an important problem for electric vehicle applications. The paper discusses a solution to this problem. In this region, an inverter can use a different PWM method to keep the NPP ripple within the desired limits. The proposed PWM method uses only the large and zero vectors to operate the inverter. Therefore, the neutral point current is kept at zero, and the NPP ripple is minimized.

Moreover, the paper makes a comparison between the capacitor sizes of 2L-VSI and 3L-NPC inverters for the PMaSynRM. It is noted that the capacitor size of the 3L-NPC inverter depends heavily on fundamental frequency; on the other hand, the capacitor size of 2L-VSI depends heavily on the switching frequency. Due to this effect, increasing the fundamental frequency provides a capacitor size reduction benefit for the 3L-NPC inverter while making minimal change in the capacitor size of 2L-VSI. The results show that the required capacitance for 2L-VSI is 60% lower than 3L-NPC inverter size considering the NTV method is applied to the 3L-NPC inverter. It is important to mention that there are two capacitors in the 3L-NPC inverter so the voltage rating of the capacitors for 3L-NPC VSI is half that of the 2L-VSI. However, capacitors of a 3L-NPC inverter are expected to have a total larger volume and larger weight than 2L-VSI. Inverter designers should pay attention to this difference. It is proven that having a larger fundamental frequency or having a larger power factor decreases the required DC-link capacitor for the 3L-NPC inverter. Therefore, the gap between the DC-link capacitor sizes of 2L-VSI and 3L-NPC inverter is reducing under certain design conditions.

Another important point is the allowed NPP ripple and DC-link ripple values. A high NPP ripple is expected to cause higher stress on the switches and a slight increase in the output THD. However, the main limiting factor of the NPP ripple is the voltage-blocking capabilities of the power switches. If 600 V switches are used and we decide to limit switch voltage by 450 V, we may let the neural point have a 100 V peak–peak voltage ripple. In that condition, each DC-link capacitor can be around 130–270 μF range. On the other hand, increasing the applied voltage to the switches decreases their reliability and lifetime.

This study shows that the DC-link capacitor sizing of a 3L-NPC should be integrated within the design step. To increase the performance of NPP ripple control, a combination of NPP control modulations with the power factor correcting modulation techniques can be identified as a future research point. Similarly, it can also be concluded that the switching losses associated with different NPP control methods also need special consideration.

The characteristics of a PMaSynRM are assumed in this study. The findings can differ for another drive system, such as an IPMSM drive. A higher power factor in base speed is going to be a definite advantage for the IPMSM. However, IPMSMs can have leading power factors in the field weakening region. In [23], NPP control with leading power factors is targeted for an IPMSM drive. As a future work, capacitor sizing can be extended for operating points with a leading power factor.

AUTHOR CONTRIBUTIONS

Serhat Emir Ogan: Conceptualization; data curation; formal analysis; investigation; methodology; validation; visualization; writing—original draft. **Emine Bostanci**: Conceptualization; methodology; resources; supervision; writing—original draft.

ACKNOWLEDGEMENTS

This work was supported in part by the Scientific and Technological Research Council of Turkey under Grant 121E729.

CONFLICT OF INTEREST STATEMENT

The authors declare no conflicts of interest.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

ORCID

Emine Bostanci https://orcid.org/0000-0002-3047-6953

REFERENCES

1. Husain, I., Ozpineci, B., Islam, M.S., Gurpinar, E., Su, G.J., Yu, W., et al.: Electric drive technology trends, challenges, and opportunities for future electric vehicles. Proc. IEEE 109, 1039–1059 (2021)
2. Reimers, J., Dorn-Gomba, L., Mak, C., Emadi, A.: Automotive traction inverters: Current status and future trends. IEEE Trans. Veh. Technol. 68, 3337–3350 (2019)
3. Orfanoudakis, G.I., Sharkh, S.M., Yuratich, M.A., Abusara, M.A.: Loss comparison of two and three-level inverter topologies. In: Proceedings of the 5th IET International Conference on Power Electronics, Machines and Drives (PEMD 2010), pp. 1–6. IEEE, Piscataway, NJ (2010)
4. Schweizer, M., Friedli, T., Kolar, J.W.: Comparative evaluation of advanced three-phase three-level inverter/converter topologies against two-level systems. IEEE Trans. Ind. Electron. 60, 5515–5527 (2013)
5. Teichmann, R., Bernet, S.: A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications. IEEE Trans. Ind. Appl. 41, 855–865 (2005)
6. Madan, A., Bostanci, E.: Comparison of two-level and three-level NPC inverter topologies for a PMSM drive for electric vehicle applications, pp. 147–154. IEEE, Piscataway, NJ (2019)
7. Welchko, B.A., Correa, M.B.D.R., Lipo, T.A.: A three-level MOSFET inverter for low-power drives. IEEE Trans. Ind. Electron. 51, 669–674 (2004)
8. Masisi, L., Pillay, P., Williamson, S.S.: A three-level neutral-point-clamped inverter synchronous reluctance machine drive. IEEE Trans. Ind. Appl. 51, 4531–4540 (2015)
9. Jayakumar, V., Chokkalingam, B., Munda, J.L.: A comprehensive review on space vector modulation techniques for neutral point clamped multi-level inverters. IEEE Access 9, 112104–112144 (2021)
10. Woldegiorgis, D., Wei, Y., Mhiesan, H., Mantooth, A.: A new DC-link capacitor voltage balancing method for three-level SVM strategies based on two-level space vector diagram. In: Proceedings of 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), pp. 1746–1751. IEEE, Piscataway, NJ (2020)
11. Gu, M., Wang, Z., Dordevic, O.: Analysis and reduction of current and voltage ripple in DC link for three-level NPC inverter-fed dual three-phase motor drives. IEEE Trans. Power Electron. 38, 5128–5140 (2023)
12. Zorig, A., Barkat, S., Sangwongwanich, A.: Neutral point voltage balancing control based on adjusting application times of redundant vectors for three-level NPC inverter. IEEE J. Emerging Sel. Top. Power Electron. 10, 5604–5613 (2022)
13. An, S.W., Kim, S.M., Lee, K.B.: Optimized space-vector modulation to reduce neutral point current for extending capacitor lifetime in three-level inverters. IEEE Access 8, 97689–97697 (2020)
14. Zhao, Z., Diao, F., Wu, Y., Wang, Z., Zhao, Y.: DC-link capacitor current modeling and analysis for three-level voltage source inverters. In: Proceedings of 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 2434–2439. IEEE, Piscataway, NJ (2021)
15. Jain, S., Kishore, N., Shukla, K.: Comparison of various PWM techniques for DC link capacitors voltage balancing of a three-level NPC VSI. In: Proceedings of the 2021 International Conference on Intelligent Technologies (CONIT), pp. 1–6. IEEE, Piscataway, NJ (2022)
16. Ozkan, Z., Hava, A.M.: DC-bus ripple current characterization of three-phase 2/3l-VSIS considering the spectral characteristics. In: Proceedings of the 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), pp. 667–674. IEEE, Piscataway, NJ (2015)
17. Masisi, L., Pillay, P., Williamson, S.S.: Three level NPC inverter DC capacitor sizing for a synchronous reluctance machine drive. In: Proceediongs of the 2014 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 2925–2931. IEEE, Piscataway, NJ (2014)
18. Pou, J., Pindado, R., Boroyevich, D., Rodríguez, P.: Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter. IEEE Trans. Ind. Electron. 52, 1582–1588 (2005)
19. Jiang, W., Huang, X., Wang, J., Wang, J., Li, J.: A carrier-based pwm strategy providing neutral-point voltage oscillation elimination for multi-phase neutral point clamped 3-level inverter. IEEE Access 7, 124066–124076 (2019)
20. Xue, V.: Center-Aligned SVPWM Realization for 3-Phase 3-Level Inverter. Application Report SPRABS6. Texas Instruments, Dallas, TX (2012)
21. Pou, J., Pindado, R., Boroyevich, D., Rodríguez, P.: Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter. IEEE Trans. Ind. Electron. 52, 1582–1588 (2005)
22. Ayhan, U., Hava, A.M.: Analysis and characterization of dc bus ripple current of two-level inverters using the equivalent centered harmonic approach. In: Proceedings of the 2011 IEEE Energy Conversion Congress and Exposition, pp. 3830–3837. IEEE, Piscataway, NJ (2011)
23. Choudhury, A., Pillay, P.: Space vector based capacitor voltage balancing for a three-level NPC traction inverter drive. IEEE J. Emerging Sel. Top. Power Electron. 8, 1276–1286 (2020)

How to cite this article: Ogan, S.E., Bostanci, E.: Capacitor sizing of three-level neutral point clamped voltage source inverter for electric vehicles: Effects of modulation and motor characteristics. IET Power Electron. 1–16 (2024). https://doi.org/10.1049/pel2.12665